CgC

PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

August 10, 2005
Date

Alexandra Beggs
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	: Timothy B. Cowles, Brian M. Shirley and Greg A. Blodgett	Attorney Docket No.:	501030.01
Patent No.	: US 6,771,553 B2	Serial No.	: 10/056,935
Issue Date	: August 3, 2004	Filed	: October 18, 2001
Title	: LOW POWER AUTO-REFRESH CIRCUIT AND METHOD FOR DYNAMIC RANDOM ACCESS MEMORIES		

REQUEST FOR CERTIFICATE OF CORRECTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

A Certificate of Correction under 35 U.S.C. § 254 is respectfully requested for the above-identified patent in order to correct Patent and Trademark Office errors made during the printing of the patent. The changes in the patent needed to correct the errors are as follows:

Column, Line	Reads	Should Read
Column 2, Line 49	"spurious command"	--spurious commands--
Column 6, Lines 1-6	"After the input buffers **110** are enabled by a high IBENCLK signal, the IBENCMD signal transitions high to switch the input buffers **110** to a low	--After the input buffers **110** are enabled by a high IBENCLK signal, the IBENCMD signal transitions high to switch the input buffers **110** to a low impendance state and to turn OFF the

impedance state and to turn OFF the transistors **130-136** so they do not affect the at time T_0 and registered at time T_1 by the rising edge of the external clock CLK signal."

transistors **130-136** so they do not affect the operation of the power saving circuit **100**. When the input buffers **110** are switched to a high impedance state by a low IBENCLK signal, the transistors **130-136** are turned ON to bias high respective internal command signal lines to which they are coupled.

The internal command signals IRAS*, ICAS*, IWE*, and ICS*, as well as other internal command signals from the input buffers **110,** are applied to a command decoder unit **140**. The command decoder unit **140** generates a plurality of memory commands, including an auto-refresh command AREF, from various combinations of the command signals applied to its inputs. As explained above, the AREF command is asserted responsive to decoding IRAS*, ICAS*, and ICS* active low and IWE* inactive high.

The auto-refresh command AREF is applied to a refresh decoder **150** along with the internal clock ICLK signal and the internal clock enable ICKE signal. Based on the state of the ICKE signal, the refresh decoder **150** determines if the AREF command is for an auto-refresh or if it is for

a self-refresh. If ICKE is high, the AREF command is interpreted as an auto-refresh command, in which case the refresh decoder **150** passes the AREF command to an output terminal as an AREF' command. If ICKE is low, the AREF command is interpreted as a self-refresh command, in which case the refresh decoder **150** generates a SREF command. The refresh decoder **150** command will continue to generate the SREF command until the ICKE signal transitions high.

The AREF command is also applied to a timer **154**, which generates a T_{OUT} pulse after a predetermined period. The T_{OUT} pulse causes the refresh decoder **150** to terminate the AREF' command, thereby terminating the auto-refresh cycle.

All of the input buffers **110, 120, 124** as well as the transistors **130-136**, the inverter **138,** the command decoder unit **140**, the refresh decoder **150** and the timer **154**, are shown in FIG. **2** as being located in the command decoder **4**. However, as previously mentioned, these components could alternatively be located elsewhere in the SDRAM **2** or in other memory devices.

The operation of the power saving circuit **100** will now be explained with reference to the timing diagram of FIG. **3**. The combination of control signals ("CMD") that constitute an auto-refresh AREF command are applied to the SDRAM **2** at time T_0 and registered at time T_1 by the rising edge of the external clock CLK signal.--

Column 7, Lines 14-66	"The operation of the power saving circuit **200** is substantially the same as the power saving circuit **100**. Specifically, in response to registering an AREF command, the IBENCMD, IBENADD and IBENCLK signals transition low to disable the input buffers **102, 110** and the internal clock buffer **230**. As a result, neither the input buffers **102, 110** nor circuitry (not shown) downstream from the internal clock buffer **230** consume power during the auto-refresh cycle initiated in response to the operation of the power saving circuit **100**. When the input buffers **110** are switched to a high impedance state by a low IBENCLK signal, the transistors **130-136** are turned	--The operation of the power saving circuit **200** is substantially the same as the power saving circuit **100**. Specifically, in response to registering an AREF command, the IBENCMD, IBENADD and IBENCLK signals transition low to disable the input buffers **102, 110** and the internal clock buffer **230**. As a result, neither the input buffers **102, 110** nor circuitry (not shown) downstream from the internal clock buffer **230** consume power during the auto-refresh cycle initiated in response to the AREF command.--

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Column 16, Line 59	"and coupled thorough"	--and coupled through--
Column 17, Line 8	"to removing"	--to remove--
Column 18, Lines 3	"decoder"	--decode--

and 6

Column 18, Line 21	"coupled thorough"	--coupled through--
Column 19, Line 22	"claim **63**"	--claim **62**--
Column 22, Line 4	"claim **89**"	--claim **88**--

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The Commissioner is hereby authorized to charge payment of any fees associated with this communication to Deposit Account No. 50-1266. A duplicate copy of this sheet is enclosed.

Favorable consideration of this Request is respectfully requested.

Respectfully submitted,

Date: August 8, 2005 By: _____

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All of the input buffers **110, 120, 124** as well as the transistors **130-136**, the inverter **138,** the command decoder unit **140**, the refresh decoder **150** and the timer **154**, are shown in FIG. **2** as being located in the command decoder **4**. However, as previously mentioned, these components could alternatively be located elsewhere in the SDRAM **2** or in other memory devices.

The operation of the power saving circuit **100** will now be explained with reference to the timing diagram of FIG. **3**. The combination of control signals ("CMD") that constitute an auto-refresh AREF command are applied to the SDRAM **2** at time T_0 and registered at time T_1 by the rising edge of the external clock CLK signal.--

Column 7, Lines 14-66	"The operation of the power saving circuit **200** is substantially the same as the power saving circuit **100**. Specifically, in response to registering an AREF command, the IBENCMD, IBENADD and IBENCLK signals transition low to disable the input buffers **102, 110** and the internal clock buffer **230**. As a result, neither the input buffers **102, 110** nor circuitry (not shown) downstream from the internal clock buffer **230** consume power during the auto-refresh cycle initiated in response to the operation of the power saving circuit **100**. When the input buffers **110** are switched to a high impedance state by a low IBENCLK signal, the transistors **130-136** are turned	--The operation of the power saving circuit **200** is substantially the same as the power saving circuit **100**. Specifically, in response to registering an AREF command, the IBENCMD, IBENADD and IBENCLK signals transition low to disable the input buffers **102, 110** and the internal clock buffer **230**. As a result, neither the input buffers **102, 110** nor circuitry (not shown) downstream from the internal clock buffer **230** consume power during the auto-refresh cycle initiated in response to the AREF command.--

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PATENT NO. : US 6,771,553 B2
DATED : August 3, 2004
INVENTOR(S) : Timothy B. Cowles, Brian M. Shirley and Greg A. Blodgett

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The auto-refresh command AREF is applied to a refresh decoder **150** along with the internal clock ICLK signal and the internal clock enable ICKE signal. Based on the state of the ICKE signal, the refresh decoder **150** determines if the AREF command is for an auto-refresh or if it is for a self-refresh. If ICKE is high, the AREF command is interpreted as an auto-refresh command, in which case the refresh decoder **150** passes the AREF command to an output terminal as an AREF' command. If ICKE is low, the AREF command is interpreted as a self-refresh command, in which case the refresh decoder **150** generates a SREF command. The refresh decoder **150**

command will continue to generate the SREF command until the ICKE signal transitions high.

The AREF command is also applied to a timer **154**, which generates a T_{OUT} pulse after a predetermined period. The T_{OUT} pulse causes the refresh decoder **150** to terminate the AREF' command, thereby terminating the auto-refresh cycle.

All of the input buffers **110, 120, 124** as well as the transistors **130-136**, the inverter **138,** the command decoder unit **140**, the refresh decoder **150** and the timer **154**, are shown in FIG. **2** as being located in the command decoder **4**. However, as previously mentioned, these components could alternatively be located elsewhere in the SDRAM **2** or in other memory devices.

The operation of the power saving circuit **100** will now be explained with reference to the timing diagram of FIG. **3**. The combination of control signals ("CMD") that constitute an auto-refresh AREF command

		are applied to the SDRAM **2** at time T_0 and registered at time T_1 by the rising edge of the external clock CLK signal.--
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Column 7, Lines 14-66	"The operation of the power saving circuit **200** is substantially the same as the power saving circuit **100**. Specifically, in response to registering an AREF command, the IBENCMD, IBENADD and IBENCLK signals transition low to disable the input buffers **102, 110** and the internal clock buffer **230**. As a result, neither the input buffers **102, 110** nor circuitry (not shown) downstream from the internal clock buffer **230** consume power during the auto-refresh cycle initiated in response to the operation of the power saving circuit **100**. When the input buffers **110** are switched to a high impedance state by a low IBENCLK signal, the transistors **130-136** are turned ON to bias high respective internal command signal lines to which they are coupled. The internal command signals IRAS*, ICAS*, IWE*, and ICS*, as well	--The operation of the power saving circuit **200** is substantially the same as the power saving circuit **100**. Specifically, in response to registering an AREF command, the IBENCMD, IBENADD and IBENCLK signals transition low to disable the input buffers **102, 110** and the internal clock buffer **230**. As a result, neither the input buffers **102, 110** nor circuitry (not shown) downstream from the internal clock buffer **230** consume power during the auto-refresh cycle initiated in response to the AREF command.--

as other internal command signals from the input buffers **110,** are applied to a command decoder unit **140**. The command decoder unit **140** generates a plurality of memory commands, including an auto-refresh command AREF, from various combinations of the command signals applied to its inputs. As explained above, the AREF command is asserted responsive to decoding IRAS*, ICAS*, and ICS* active low and IWE* inactive high.

The auto-refresh command AREF is applied to a refresh decoder **150** along with the internal clock ICLK signal and the internal clock enable ICKE signal. Based on the state of the ICKE signal, the refresh decoder **150** determines if the AREF command is for an auto-refresh or if it is for a self-refresh. If ICKE is high, the AREF command is interpreted as an auto-refresh command, in which case the refresh decoder **150** passes the AREF command to an output terminal as an AREF' command. If

ICKE is low, the AREF command is interpreted as a self-refresh command, in which case the refresh decoder **150** generates a SREF command. The refresh decoder **150** command will continue to generate the SREF command until the ICKE signal transitions high.

The AREF command is also applied to a timer **154**, which generates a T_{OUT} pulse after a predetermined period. The T_{OUT} pulse causes the refresh decoder **150** to terminate the AREF' command, thereby terminating the auto-refresh cycle.

All of the input buffers **110, 120, 124** as well as the transistors **130-136**, the inverter **138** the command decoder unit **140**, the refresh decoder **150** and the timer **154**, are shown in FIG. **2** as being located in the command decoder **4**. However, as previously mentioned, these components could alternatively be located elsewhere in the SDRAM **2** or in other memory devices.

The operation of the power saving circuit **100**

	will now be explained with reference to the timing diagram of FIG. **3**. The combination of control signals ("CMD") that constitute an auto-refresh AREF command are applied to the SDRAM **2** AREF command."	
Column 8, Line 41	"("0" for full AREF period)"	--"0" (for full AREF period)--
Column 8, Line 54	"when the AREF command"	--when the AREF command is asserted--
Column 8, Lines 56 and 62	"to end of the"	--to end the--
Column 10, Line 23	"operable to removing"	--operable to remove--
Column 11, Line 54	"and a detecting"	--and detecting a--
Column 12, Line 37	"transition terminate"	--transition to terminate--
Column 13, Lines 3 and 5	"and decoder"	--and decode--
Column 13, Line 17	"coupled thorough"	--coupled through--
Column 14, Line 64	"coupled thorough"	--coupled through--
Column 16, Lines 43 and 46	"decoder"	--decode--
Column 16, Line 59	"and coupled thorough"	--and coupled through--
Column 17, Line 8	"to removing"	--to remove--
Column 18, Lines 3 and 6	"decoder"	--decode--
Column 18, Line 21	"coupled thorough"	--coupled through--
Column 19, Line 22	"claim **63**"	--claim **62**--
Column 22, Line 4	"claim **89**"	--claim **88**--

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Patent No. US 6,771,553 B2

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AUG 2 2 2005